

ABSTRACT OF THE DISCLOSURE

A process wherein an insulating region is formed in a body at least around an array portion of a semiconductor body; a gate electrode of semiconductor material is formed on top of a circuitry portion of the semiconductor body; a first silicide protection mask is formed on top of the array portion; the gate electrode and the active areas of the circuitry portion are silicided and the first silicide protection mask is removed. The first silicide protection mask (is of polysilicon and is formed simultaneously with the gate electrode. A second silicide protection mask of dielectric material covering the first silicide protection mask is formed before silicidation of the gate electrode. The second silicide protection mask is formed simultaneously with spacers formed laterally to the gate electrode.

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